Table 1-1 Instruction Operation (continued on following 4 pages)

Address Mode	Note	Cycle	Address Bus	Data Bus	RWB
1a. Absolute !abs ADC, AND, CMP, EOR, MOV, OR, SBC 14 OpCodes, 3 bytes, 4 and 5 cycles	 (1)	1 2 3 4 4a	PC PC+1 PC+2 AA AA	OpCode AAL AAH Data Data	1 1 1 1 0
1b. Absolute !abs CALL 1 OpCode, 3 bytes, 8 cycles		1 2 3 4 5 6 7 8 1	PC PC+1 PC+2 SP SP SP-1 SP-1 SP-1 New PC	OpCode New PCL New PCH IO PCH PCL IO IO Next OpCode	1 1 1 1 0 0 1 1 1
1c. Absolute !abs JMP 1 OpCode, 3 bytes, 3 cycles		1 2 3 1	PC PC+1 PC+2 New PC	OpCode New PCL New PCH Next OpCode	1 1 1 1
1d. Absolute (R-M-W) !abs ASL, DEC, INC, LSR, ROL, ROR 6 OpCodes, 3 bytes, 5 cycles		1 2 3 4 5	PC PC+1 PC+2 AA AA	OpCode AAL AAH Data Data	1 1 1 1 0
1e. Absolute (R-M-W) !abs TCLR1, TSET1 2 OpCodes, 3 bytes, 6 cycles		1 2 3 4 5 6	PC PC+1 PC+2 AA AA AA	OpCode AAL AAH Data Data Data	1 1 1 1 1 0
2. Absolute Indexed Indirect (!abs+x) JMP 1 OpCode, 3 bytes, 6 cycles		1 2 3 4 5 6 1	PC PC+1 PC+2 PC+2 AA+X AA+X+1 New PC	OpCode AAL AAH IO New PCL New PCH Next OpCode	1 1 1 1 1 1 1
3. Absolute, X !abs+x ADC, AND, CMP, EOR, MOV, OR, SBC 8 OpCodes, 3 bytes, 5 and 6 cycles	 (1)	1 2 3 4 5 5a	PC PC+1 PC+2 PC+2 AA+X AA+X	OpCode AAL AAH IO Data Data	1 1 1 1 1 0
4. Absolute, Y !abs+y ADC, AND, CMP, EOR, MOV, OR, SBC 8 OpCodes, 3 bytes, 5 and 6 cycles	 (1)	1 2 3 4 5 5a	PC PC+1 PC+2 PC+2 AA+Y AA+Y	OpCode AAL AAH IO Data Data	1 1 1 1 1 0

Table 1-1 (continued)

Address Mode	Note	Cycle	Address Bus	Data Bus	RWB
5. Accumulator ASL, DEC, INC, LSR, ROL, ROR 6 OpCodes, 1 byte, 2 cycles		1 2	PC PC+1	OpCode [PC+1]	1 1
6a. Direct dp ADC, AND, CMP, EOR, MOV, OR, SBC 14 OpCodes, 2 bytes, 3 and 4 cycles	 (1)	1 2 3 3a	PC PC+1 DO DO	OpCode DO Data Data	1 1 1 0
6b. Direct (R-M-W) dp ASL, DEC, INC, LSR, ROL, ROR, CLR1, SET1 22 OpCodes, 2 bytes, 4 cycles		1 2 3 4	PC PC+1 DO DO	OpCode DO Data Data	1 1 1 0
6c. Direct dp CMPW 1 OpCode, 2 bytes, 4 cycles		1 2 3 4	PC PC+1 DO DO+1	OpCode DO Data Low Data High	1 1 1 1
6d. Direct dp ADDW, MOVW, SUBW 4 OpCodes, 2 bytes, 5 cycles	 (8)	1 2 3 4 5	PC PC+1 DO DO DO+1	OpCode DO Data Low Data Low Data High	1 1 1 0/1 0/1
6e. Direct (R-M-W) dp DECW, INCW 2 OpCodes, 2 bytes, 6 cycles		1 2 3 4 5 6	PC PC+1 DO DO DO+1 DO+1	OpCode DO Data Low Data Low Data High Data High	1 1 1 0 1 0
7a. Direct Direct dp,dp ADC, AND, CMP, EOR, OR, SBC 6 OpCodes, 3 bytes, 6 cycles	 (7)	1 2 3 4 5 6	PC PC+1 DO PC+2 DO DO	OpCode DO Data DO Data Data	1 1 1 1 1 0/1
7b. Direct Direct dp,dp MOV 1 OpCode, 3 bytes, 5 cycles		1 2 3 4 5	PC PC+1 DO PC+2 DO	OpCode DO Data DO Data	1 1 1 1 0
8. Direct Immediate dp,#imm ADC, AND, CMP, EOR, MOV, OR, SBC 7 OpCodes, 3 bytes, 5 cycles	 (7)	1 2 3 4 5	PC PC+1 PC+2 DO DO	OpCode Data DO Data Data	1 1 1 1 0/1
9. Direct Indexed Indirect [dp+x] ADC, AND, CMP, EOR, MOV, OR, SBC 8 OpCodes, 2 bytes, 6 and 7 cycles	 (1)	1 2 3 4 5 6 6a	PC PC+1 PC+1 DO+X DO+X+1 AA AA	OpCode DO IO AAL AAH Data Data	1 1 1 1 1 1 0

Table 1-1 (continued)

Address Mode	Note	Cycle	Address Bus	Data Bus	RWB
10. Direct Indirect Indexed [dp]+y ADC, AND, CMP, EOR, MOV, OR, SBC 8 OpCodes, 2 bytes, 6 and 7 cycles		1 2 3 4 5 6 (1)	PC PC+1 DO DO+1 DO+1 AA AA	OpCode DO AAL AAH IO Data Data	1 1 1 1 1 1 0
11. Direct Relative dp, rel BBC, BBS, CBNE, DBNZ 18 OpCodes, 2 bytes, 5 and 7 cycles	(9) (2) (2)	1 2 3 4 5 5a 5b	PC PC+1 DO DO PC+2 PC+2 PC+2	OpCode DO Data Data Offset IO IO	1 1 1 0/1 1 1 1
12a. Direct, X dp+x ADC, AND, CMP, EOR, MOV, OR, SBC 10 OpCodes, 2 bytes, 4 and 5 cycles	(1)	1 2 3 4 4a	PC PC+1 PC+1 DO+X DO+X	OpCode DO IO Data Data	1 1 1 1 0
12b. Direct, X (R-M-W) dp+x ASL, DEC, INC, LSR, ROL, ROR 6 OpCodes, 2 bytes, 5 cycles		1 2 3 4 5	PC PC+1 PC+1 DO+X DO+X	OpCode DO IO Data Data	1 1 1 1 0
12c. Direct, X Relative dp+x, rel CBNE 1 OpCode, 3 bytes, 6 and 8 cycles	(2) (2)	1 2 3 4 5 6 6a 6b	PC PC+1 PC+1 DO+X DO+X PC+2 PC+2 PC+2	OpCode DO IO Data IO Offset IO IO	1 1 1 1 1 1 1 1
13. Direct, Y dp+y MOV 2 OpCodes, 2 bytes, 4 and 5 cycles	(1)	1 2 3 4 4a	PC PC+1 PC+1 DO+Y DO+Y	OpCode DO IO Data Data	1 1 1 1 0
14a. Indirect (x) ADC, AND, CMP, EOR, MOV, OR, SBC 8 OpCodes, 1 byte, 3 and 4 cycles	(1)	1 2 3 3a	PC PC+1 X X	OpCode [PC+1] Data Data	1 1 1 0
14b. Indirect (x)+ MOV 2 OpCodes, 1 byte, 4 cycles	(5) (6)	1 2 3 4	PC PC+1 X X	OpCode [PC+1] Data Data	1 1 1 0/1
15. Indirect Indirect (x),(y) ADC, AND, CMP, EOR, OR, SBC 6 OpCodes, 1 byte, 5 cycles	(7)	1 2 3 4 5	PC PC+1 Y X X	OpCode [PC+1] Data Data Data	1 1 1 1 0/1

Table 1-1 (continued)

Address Mode	Note	Cycle	Address Bus	Data Bus	RWB
16. Immediate #imm ADC, AND, CMP, EOR, MOV, OR, SBC 11 OpCodes, 2 bytes, 2 cycles		1 2	PC PC+1	OpCode Data	1 1
17. Implied i CLRC, CLRP, CLRV, DAA, DAS, DEC, DI, DIV, EI, INC, MOV, MUL, NOP, NOTC, SETC, SETP, XCN 24 OpCodes, 1 byte, 2, 3, 5, 9 and 12 cycles		1 2 X	PC PC+1 PC+1	OpCode [PC+1] IO	1 1 1
18a. Bit mem.bit AND1, EOR1, MOV1, OR1 6 OpCodes. 3 bytes, 4 and 5 cycles	 (3)	1 2 3 4 4a	PC PC+1 PC+2 AA AA	OpCode AAL AAH Data IO	1 1 1 1 1
18b. Bit mem.bit MOV1, NOT1 2 OpCode, 3 bytes, 5 and 6 cycles	 (4)	1 2 3 4 4a 5	PC PC+1 PC+2 AA AA AA	OpCode AAL AAH Data IO Data	1 1 1 1 1 0
19a. Relative rel BCC, BCS, BEQ, BMI, BNE, BPL, BRA, BVC, BVS 9 OpCodes, 2 bytes, 2 and 4 cycles	 (2) (2)	1 2 2a 2b	PC PC+1 PC+1 PC+1	OpCode Offset IO IO	1 1 1 1
19b. Relative rel DBNZ 1 OpCode, 2 bytes, 4 and 6 cycles	 (2) (2)	1 2 3 4 4a 4b	PC PC+1 PC+1 PC+1 PC+1 PC+1	OpCode [PC+1] IO Offset IO IO	1 1 1 1 1 1
20a. Stack s BRK 1 OpCode, 1 byte, 8 cycles		1 2 3 4 5 6 7 8 1	PC PC+1 SP SP-1 SP-2 SP-2 VA VA+1 New PC	OpCode [PC+1] PCH PCL PSW IO New PCL New PCH Next OpCode	1 1 0 0 0 1 1 1 1
20b. Stack s RETI 1 OpCode, 1 byte, 6 cycles		1 2 3 4 5 6 1	PC PC+1 SP SP+1 SP+2 SP+3 New PC	OpCode [PC+1] IO PSW New PCL New PCH Next OpCode	1 1 1 1 1 1 1
20c. Stack s PUSH 4 OpCodes, 1 byte, 4 cycles		1 2 3 4	PC PC+1 SP SP	OpCode [PC+1] REG IO	1 1 0 1

Table 1-1 (continued)

Address Mode	Note	Cycle	Address Bus	Data Bus	RWB
20d. Stack s POP 4 OpCodes, 1 byte, 4 cycles		1 2 3 4	PC PC+1 SP SP+1	OpCode [PC+1] IO REG	1 1 1 1
20e. Stack s TCALL 16 OpCodes, 1 byte, 8 cycles		1 2 3 4 5 6 7 8 1	PC PC+1 SP SP SP-1 SP-1 VA VA+1 New PC	OpCode [PC+1] IO PCH PCL IO New PCL New PCH Next OpCode	1 1 1 0 0 1 1 1 1
20f. Stack s PCALL 1 OpCode, 2 bytes, 6 cycles		1 2 3 4 5 6 1	PC PC+1 PC+1 SP SP-1 SP-1 New PC	OpCode Offset IO PCH PCL IO Next OpCode	1 1 1 0 0 1 1
20g. Stack s RET 1 OpCode, 1 byte, 5 cycles		1 2 3 4 5 1	PC PC+1 SP SP+1 SP+2 New PC	OpCode [PC+1] IO New PCL New PCH Next OpCode	1 1 1 1 1 1

Notes: Memory is accessed every cycle.

1. Add 1 cycle for write.
2. Add 2 cycles if branch is taken.
3. Add 1 cycle for EOR1, OR1.
4. Add 1 cycle for MOV1.
5. Internal operation for MOV (X)+, A.
6. Internal operation for MOV A, (X)+.
7. Internal operation for CMP.
8. Internal operation for ADDW, SUBW and MOVW YA, dp.
9. Internal operation for BBC, BBS and CBNE.